Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDA 5100

Application Note

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2 Product Description

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2.1 Abstract

This application note describes the operation of the TDA5100 evaluation board. It demonstrates the design of a low-cost transmitter for applications in wireless I.S.M. data communication systems. A variety of application considerations are provided to assist system designers in implementing the device as a low-cost data transmitter.

The circuit board can be operated in all the modes supported by the TDA5100:

- in one of the assigned frequency bands for Short Range Devices (SRD) at either 434MHz or 869MHz
- using amplitude shift key (ASK) or frequency shift key (FSK) modulation.

The board conforms to the I-ETS 300 220 regulations.

2.2 Overview

The TDA 5100 has been implemented in a 25GHz silicon bipolar process (Siemens process “B6HF”). It supports all low power device (LPD) wireless applications with data rates of up to 100kb/s using ASK- and up to 40kb/s using FSK-digital modulation.

The basic configuration is a PLL frequency synthesizer circuit with an on-chip fully integrated VCO operating at a frequency in the 869MHz range. This frequency is divided by 64 for operation at a reference frequency of 13.5MHz or by 128 at a reference frequency of 6.8MHz.

The power amplifier is driven by the VCO with an isolation driver stage for operation at 869MHz. Operation at 434MHz is achieved by first dividing the VCO frequency by two. The power amplifier is a class C configuration. It has been optimized for high power efficiency.

Modulation is achieved by either modulating the frequency of the reference oscillator in FSK applications or by modulating the carrier amplitude using a digital output power control pin in ASK applications.

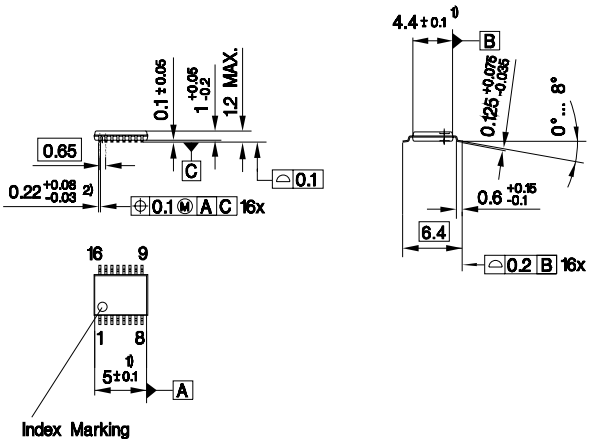
Table 2-1 summarizes the key parameters of the device:

Table 2-1 Performance Summary for the TDA5100 Transmitter

Parameter
Selectable frequency range 433-435 MHz and 868-870 MHz
Fully integrated VCO and PLL synthesizer
High efficiency power amplifier
Output power +4dBm (434MHz), +1dBm (869MHz)
Supply voltage range 2.1 V - 4.0 V
Low supply current I_S=6.9mA typ.
ASK / FSK modulation
Power down mode
Low-voltage detect function
Clock output for controller
Fast lock up time ≤1ms

2.3 Package Outlines

P-TSSOP-16



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

3 Functional Description

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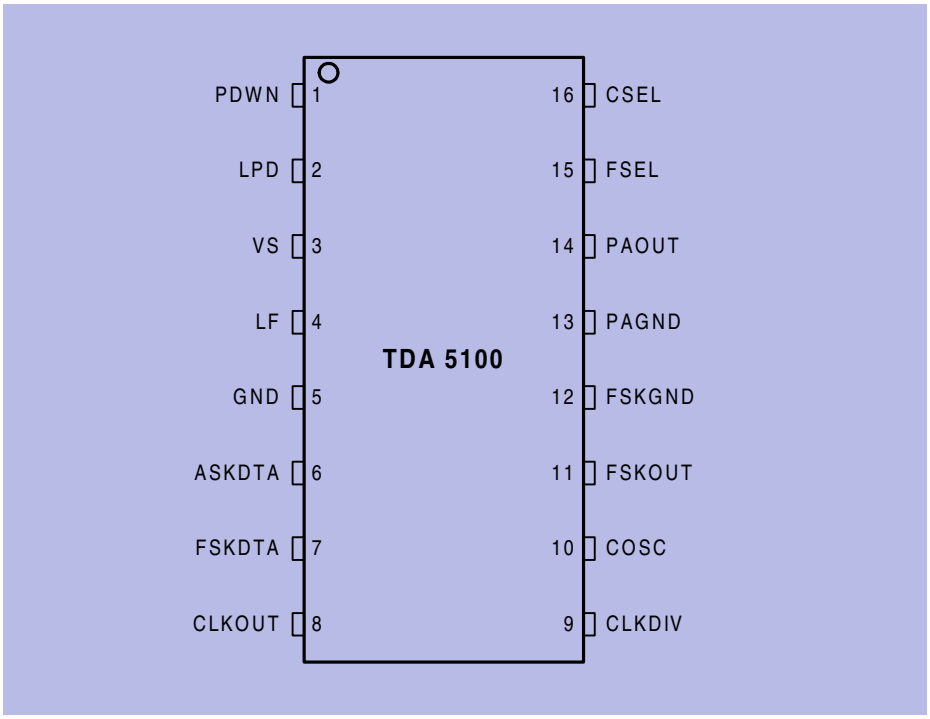
3.1 Pin Configuration

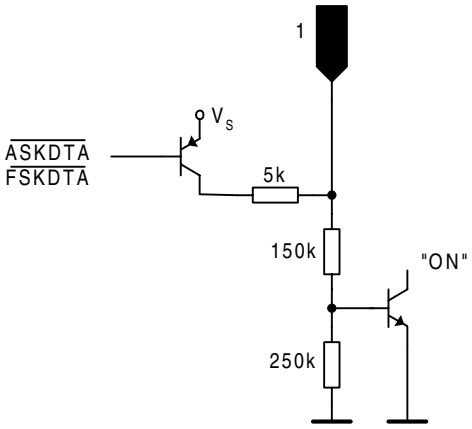
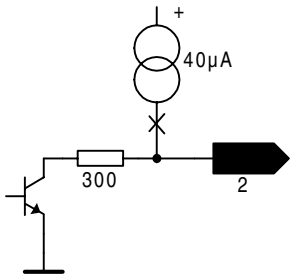
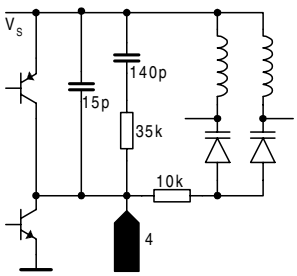


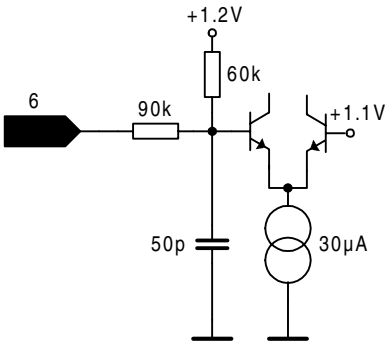
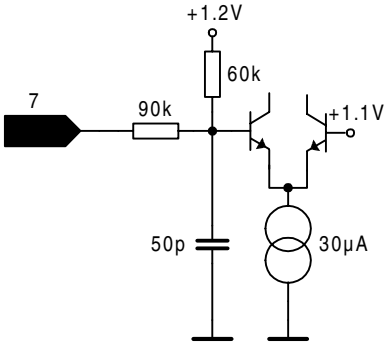
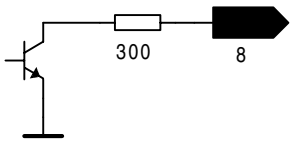
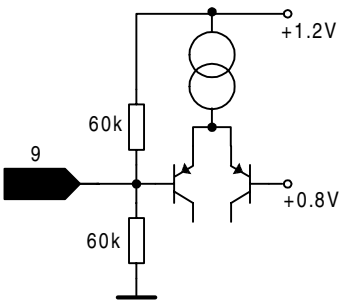
Pin_config.wmf

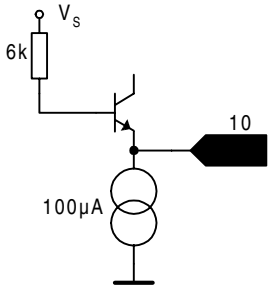
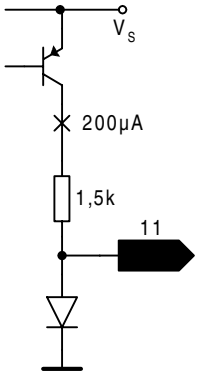
Figure 3-1 IC Pin Configuration

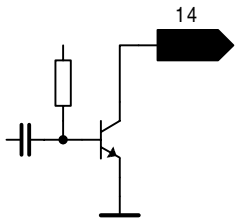
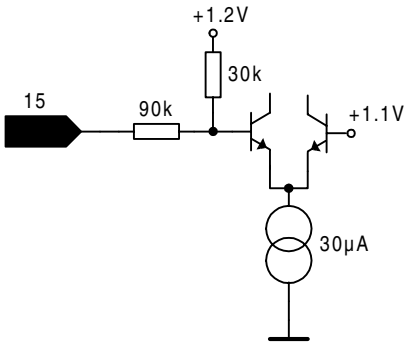
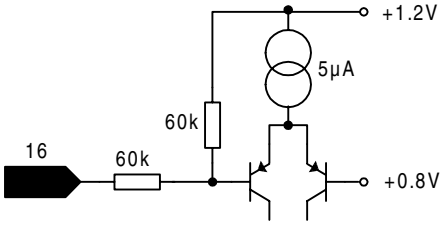
3.2 Pin Definitons and Functions

Table 3-1

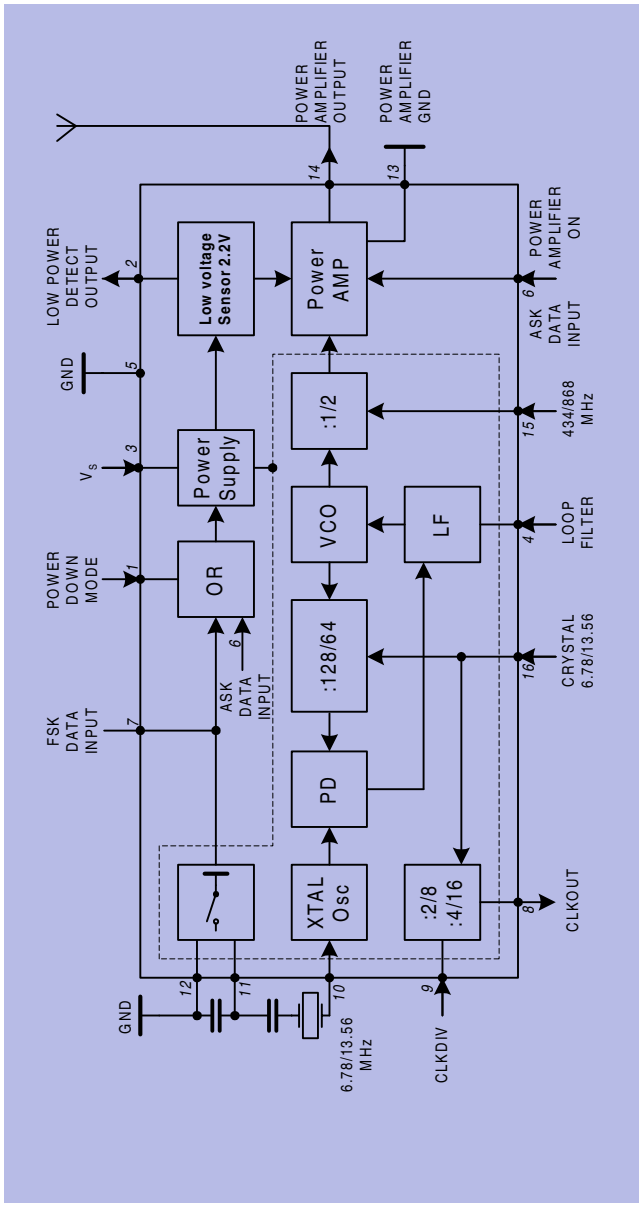
Pin No.	Symbol	Interface Schematic	Function
1	PDWN		Disable pin for transmitter circuit. PDWN < 0.7V turns off all transmitter functions. PDWN > 1.5V gives access to all transmitter functions. PDWN input will be pulled up by 40µA internally by either setting FSKDTA or ASKDTA to a logic high state.
2	LPD		This pin provides an output indicating the low-voltage state of the supply voltage VS. VS < 2.15V will set LPD to the low state. An internal pull up current of 40µA gives the output an high state at supply voltages above 2.15 V.
3	VS		This pin is used to supply DC bias to the transmitter electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground as short as possible.
4	LF		Output of the charge pump and input to the VCO control. An internal loop filter has been designed for a loop bandwidth of 150kHz. The loop bandwidth may be reduced by applying an external RC network.

5	GND		General ground connection.
6	ASKDTA		Digital amplitude modulation can be imparted to the PA through this pin. ASKDTA > 1.5V or an open enables the PA. ASKDTA < 0.5V disables the PA.
7	FSKDTA		Digital frequency modulation can be imparted to the XO by this pin. The VCO varies in accordance to the frequency of the reference oscillator. FSKDTA < 0.5V closes the FSKOUT switch at pin 11. A capacitor can be switched to the XO network this way. The XO frequency will be shifted giving the designed FSK frequency deviation. FSKDTA > 1.5V or an open will set the FSKOUT switch to a high impedance state.
8	CLKOUT		Clock output to supply a external device. A external pull up resistor has to be added in accordance to the driving requirements of the external device. A clock frequency of 3.39MHz can be selected by a logic low at CLKDIV input, pin9. A logic high or a open at the CLKDIV input will result in a CLKOUT frequency of 847.5kHz.
9	CLKDIV		This pin is used to select the desired clock division for the CLKOUT signal. A logic low CLKDIV < 0.5V selects the 339MHz output signal at pin8. A logic high CLKDIV > 1.5V or an open selects the 847.5kHz output signal.

10	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator configuration is of the negative impedance converter type. It presents a negative resistor in series to an inductor at the COSC pin.
11	FSKOUT		This pin is a switch being activated by the FSKDTA signal at pin 7. The switch is closed for a logic low at the FSKDTA pin. It is open for a logic high or a open at the FSKDTA input. FSKOUT will switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the designed FSK frequency shift of the transmitter output frequency.
12	FSKGND		Ground connection for FSK modulation output FSKOUT.
13	PAGND		Ground connection for the power amplifier (PA). All the RF ground path of the power amplifier should be concentrated to this pin.

14	PAOUT		RF output pin for the transmitter. A DC path to VS has to be supplied by the antenna matching network.
15	FSEL		This pin is used to select the desired transmitter frequency. FSEL < 0.5V will give access to the 434MHz frequency range. FSEL > 1.5V or a open will put the transmitter to the 869MHz mode.
16	CSEL		A logic low (CSEL < 0.5V) applied to this pin sets the internal frequency divider for a reference frequency of 6.7MHz. A logic high (CSEL > 1.5V or a open) will be applied for a reference frequency of 13.5MHz.

3.3 Functional Block Diagram



Funct_Block.wmf

Figure 3-2 Functional Block Diagram

4 Applications

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4.1 Antenna

The antenna used for the application board is a special loop configuration design. It utilizes an unusual capacitive loading at the end of the loop. Simulations and tests have proved this antenna to be more efficient and haveing a wider bandwidth than a conventional antenna grounded at its end. This effect is partly caused by radiation of additional electrical field components by the loop itself. The antenna in this case should not be considered as a mere magnetic loop but rather as a certain part of a dipole. Placing it apart from the electronic part on the board forms kind a of dipole antenna. The hot part of the loop - now primarily at its end - radiates certain electrical field components which add to the magnetic component.

The radiation resistance of a small loop of area A with a uniform current distribution can be calculated as

$$R_R = 320\ \pi^4\ A^2/\lambda^4$$

The inductance of a single turn loop having a circumference of U and a wire diameter of d is

$$L_L = 0.2\ U\ (\ln U/d\ -\ 1.07)$$

The unloaded $Q_U = X_L/R_R$ of such a loop is quite high in practice. The antenna configuration on the application board results in a typical *lossless*

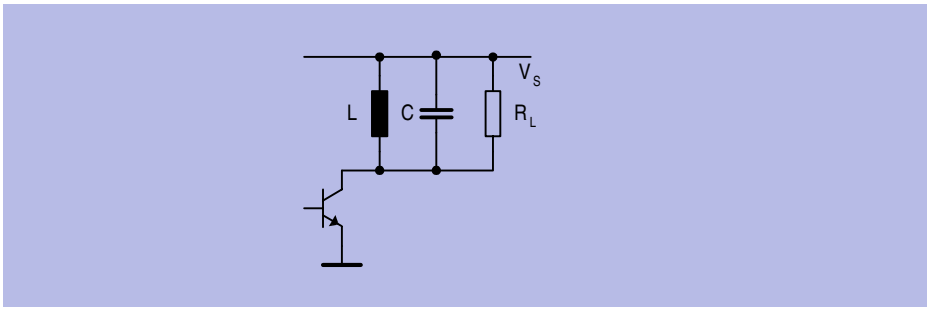
$$Q_U \approx 150\ \Omega\ /\ 9.5\ m\Omega = 15400$$

at 434Mhz. Adding the losses of the loop will reduce this value to

$$Q_U \approx 800.$$

It is at least by one order of magnitude higher then the Q of the components being used in the matching circuit. Therefore matching will be done to the losses of the components and not to R_R itself. The best matching circuit will then be the one presenting the designed load to the power amplifier while giving the highest current through L_L. The current through L_L is Q_L times the input current to the tank circuit. The loaded Q_L should be kept high in order to achieve a high antenna efficiency. Q_L should be kept down to a realistic value, however, to avoid tuning problems with a too narrow band resonance circuit.

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angel of $\Theta \leq \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 4-1. The tank circuit L//C//R_L in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.



Equivalent-power.wmf

Figure 4-1 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for "critical" operation under idealized conditions at resonance is:

$$R_{LC} = V_S^2 / 2\,P_o.$$

A typical value of R_{LC} for a RF output power of P_o= 5mW is:

$$R_{LC} = (2.7V)^2 / 10mW = 729\Omega.$$

"Critical" operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S. The high degree of efficiency under "critical" operating conditions can be explained by the low power losses at the transistor.
During the conducting phase of the transistor there will be present no or only a very small collector voltage. This way the power losses of the transistor, equal to $i_C{}^*u_{CE}$, will be minimized. This is particularly true for low current flow angels of $\Theta << \pi$.

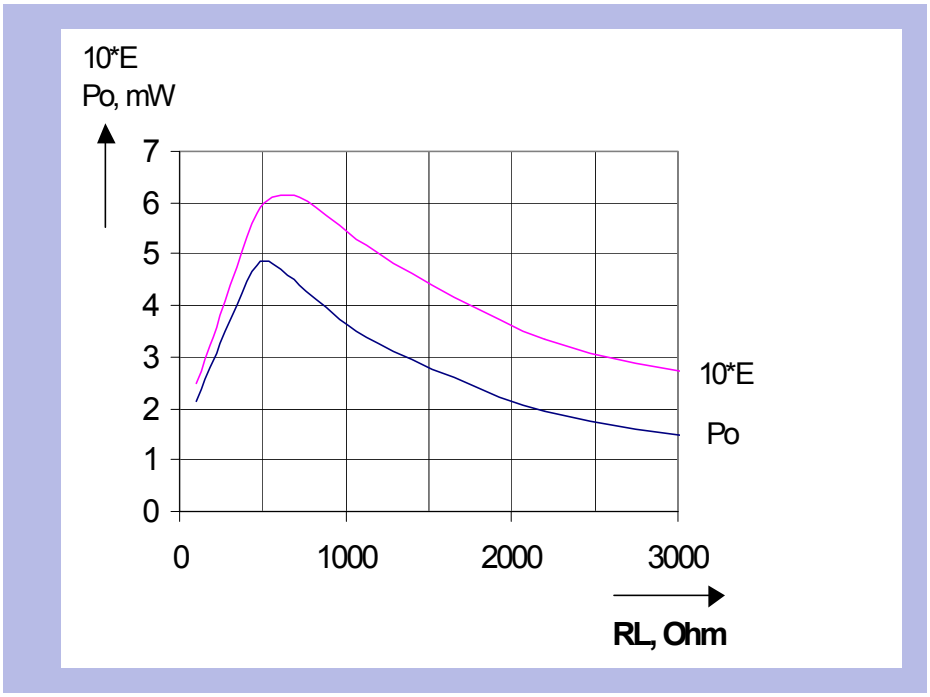
In practice the RF-saturation voltage of the PA transistor and other parasitics will reduce the "critical" R_{LC}.

The output power P_o will be reduced when operating in an “overcritical” mode at a $R_L > R_{LC}$. As shown in Figure 4-2, however, power efficiency E (and bandwidth) will increase by some degree when operating at higher R_L. The collector efficiency E is defined as

$$E = P_o / V_s * I_c$$

The diagram of Figure 4-2 has been derived from a test circuit having losses of 1.0dB within the matching network. Taking this into account, the corrected efficiency will be $E_{max} = 0.76 \cong 76\%$ at its maximum.

The DC collector current Ic of the power amplifier and the RF output power P_o vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers.



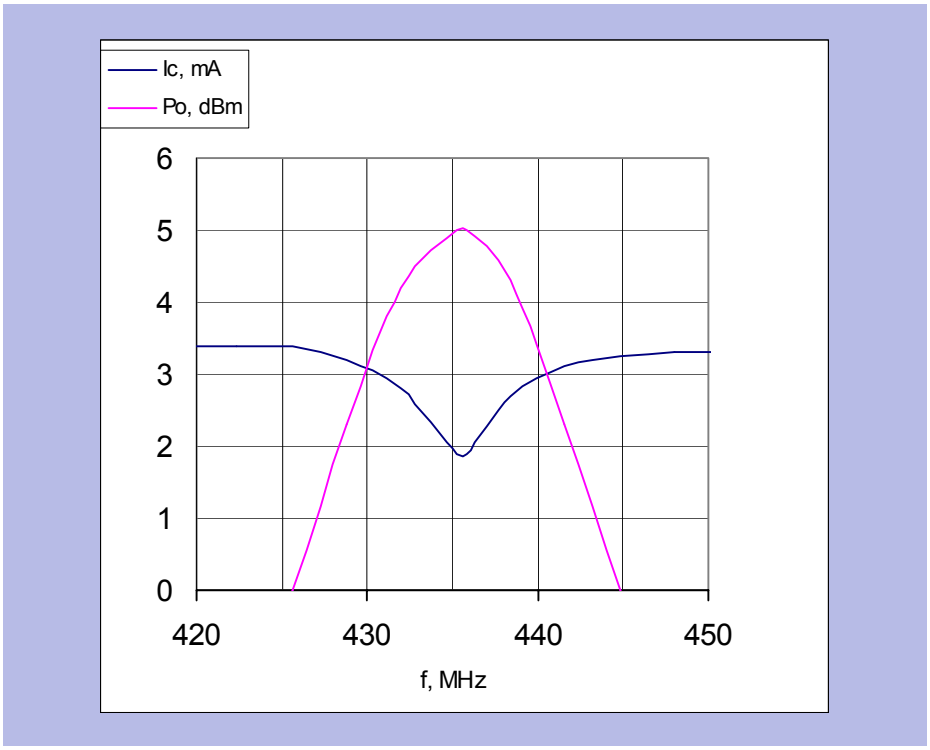
Power_output.wmf

Figure 4-2 Output power Po (mW) and collector efficiency E vs. load resistor R_L.

The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

As Figure 4-3 shows, detuning beyond the bandwidth of the antenna circuit results in a significant increase in collector current of the power amplifier and in some loss of output power. This diagram shows the data for the circuit of the test board, Figure 5-1 at the frequency of 435.4 MHz. The effective load resistor of this circuit is $R_L = 900\Omega$.

This is two times the value of a “critical” class C operation, which has been found to be $R_{LC} = 470\ \Omega$ for the PA transistor of the TDA5100 at a supply voltage of $V_S = 2.7V$.



power_vs_frq.wmf

Figure 4-3 Power output and collector current vs. frequency

The loaded Q of the antenna on the evaluation PCB ($Q_L \approx 40$ at 434MHz and $Q_L \approx 25$ at 869MHz) is quite high. A tuning-free realization requires a careful design of the components within the matching network.

The resonance frequency of the antenna circuit should be kept within its 3dB points at the operating frequency even under worst case conditions for the tolerance of the components involved. Placing the DC path for the collector voltage L1 at the end of the antenna in parallel to C3 allows some fine-tuning of the antenna by a matching L1//C3 combination.

Finding the worst case tolerances of the components will be demonstrated for an example at the more critical frequency of 434 MHz. A loaded $Q_L = 40$ corresponds to a bandwidth of:

$$B = 434MHz/Q_L = 10.8\ MHz = \pm 5.4\ MHz.$$

The resonance frequency of a LC circuit follows a $(LC)^{-1/2}$ law. Thus:

$$-\Delta f/f = \tfrac{1}{2}\ \Delta C/C = \tfrac{1}{2}\ \Delta L/L = \pm 1/2Q_L.$$

The tolerance requirements for L or C can be calculated as:

$$\Delta C/C = \Delta L/L = \pm 1/Q_L = \pm 2.5\ \%.$$

If the resonance frequency is determined equally by the C and L components, the tolerances under worst case conditions add up, resulting in a tolerance requirement for L and C of just ±1.25 % each.

The above calculation of the tolerance requirements has been done for a LC parallel tank circuit. Therefore the result directly applies to C2 of the application board. The L component of the tank circuit in the application board is formed by the combination of C3 //L1 in series to the inductance of the antenna loop . Hence, the tolerance requirements for C3 will be less stringent. A good CAE tool can help to design the antenna circuit.

The final design of C2, C3 and L1 must be done on the PCB. This empirical design is the only way to cover all the effects which influence the antenna and the matching circuit. In a first step the components given for the evaluation board may be imparted. Tuning C3 will give the characteristic drop of the DC collector current of the PA transistor at the resonance point of the tank circuit. A deeper drop will be achieved for lower values of C2. A current drop by app. 20% seems to be a good compromise for output power, power efficiency and ease of tuning. As seen in Figure 4-2, a 20% drop in collector current will be achieved by a load resistor of $R_L \approx 900\Omega$. Next, the antenna matching network requires adjusting the C3//L1 combination. A tuning free realization of the tank circuit requires a very precise loading at the end of the antenna loop. In general this can not be realized by applying just one capacitor with a standard value. Either two capacitors or a capacitor in parallel to an inductor have to be used to tune the antenna resonance precisely to the operating frequency of the transmitter. The inductance L1 should compensate a small part of the capacity C3 only. This avoids additional losses within the matching network due to the quite low Q of the inductors being used.

Suppression of the radiation of spurious harmonics may require some additional filtering within the antenna matching circuit.

The effective radiated power of the application transmitter board has been measured to be -9dBm ERP at a 434MHz frequency and –4dBm ERP at 869MHz.

The total radiated spectrum measured can be summarized as:

Table 4-1

Frequency	ERP at 434 MHz	ERP at 869 MHz	regulations, limit ETS 300 220 434/869 MHz
Carrier f_C	- 9 dBm	-4 dBm	+10 dBm
f_C + 13.5 MHz	-75 dBm	-51dBm	-36 dBm
f_C – 13.5 MHz	-73 dBm	-59 dBm	-36/-54 dBm
f_C ± 847 kHz	-62 dBm	- 67 dBm	-36 dBm
2^{nd} harmonic	-51dBm	-56 dBm	-36/-30 dBm
3^{rd} harmonic	-42 dBm	-72 dBm	-30 dBm

Utilizing higher efficiency antennas may bring up the radiated power to a level of 0 dBm ERP in both frequency bands. A very effective yet quite small antenna may be an inductively loaded stub. Its application is limited to non-handheld systems however. Absorption by a hand in close proximity will reduce its effectiveness by much more than can be observed with a magnetic antenna.

Care must be taken with all high efficiency antennas however to keep spurious radiation down below the limit level to achieve compliance with ETS 300 220. The most critical frequency under this aspect is the $f_C - f_{ref}$ component. When operated at 869MHz, it may fall into the frequency band of $\leq$ 862MHz. According to ETS 300 220, spurious emissions shall not exceed a value of -54dBm below the frequency of 862MHz.

4.2 Reference Oscillator

The transmitting frequency and its stability are determined by the reference crystal and its associated oscillator circuit.

The oscillator is of the negative impedance converter type: a resistor and a capacitor are „sign-inverted“ to give a negative resistor in series with an inductor at the oscillator port cosc pin10.

The reference oscillator either operates at 6.78MHz or at 13.56MHz. The reference frequency will be given by

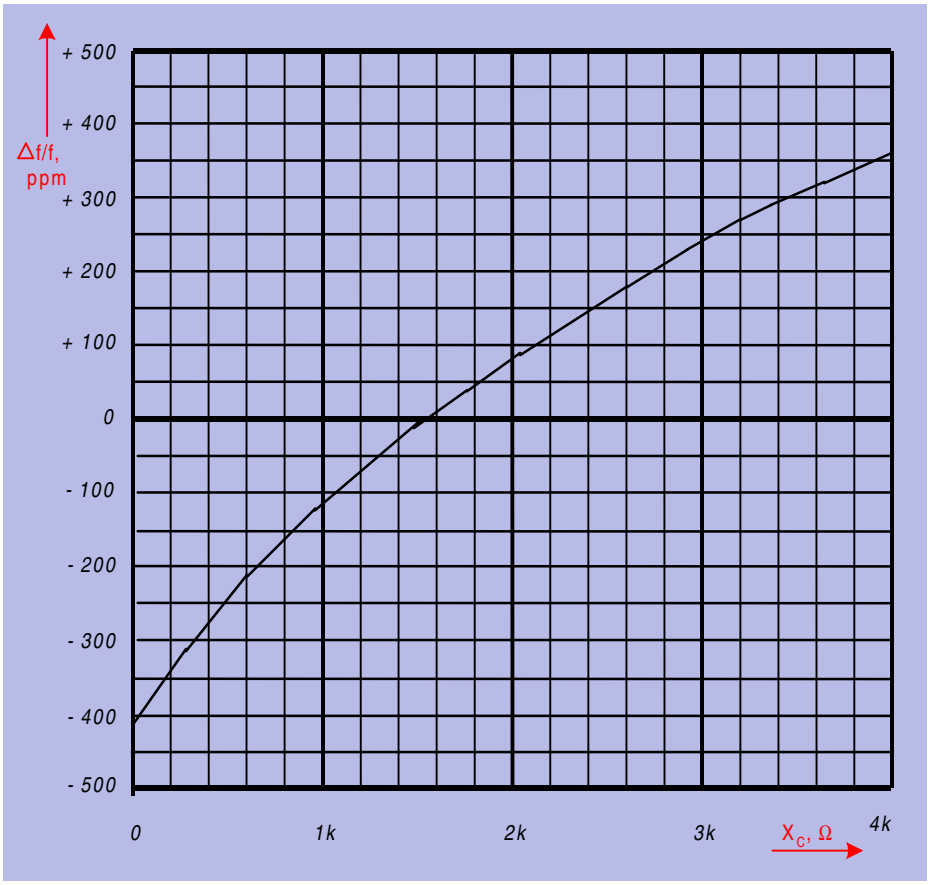
f_{ref}	CSEL input
f_{VCO} / 64	High or open
f_{VCO} / 128	Low

The transmitting frequency f_C is identical to the frequency f_{VCO} of the internal VCO for operation at 869MHz. For operation at 434MHz the frequency f_{VCO} will be divided by two, resulting in the transmitter output frequency.

The S-parameters of the oscillator circuit presented in Table 4-2 have been taken at pin10 of the TDA 5100 on the evaluation board under load conditions when oscillation just starts up. The characteristic impedance of the given S-parameters is Z_O = 1kΩ. The inductance of the equivalent input impedance varies to quite some extends with the load conditions of the oscillator however. At the operating frequency of 13.57 MHz the inductance changes from 13.94 µH under max. load conditions to 10.2 µH for a high-Q, lossless loading.

Table 4-2 S-Parameters of the Reference Oscillator

f (MHz)	S11 (Z_O=1kΩ)		Equivalent Impedance Elements	
2.0	8.64	38.8°	13.85 µH	-1184 Ω
4.0	5.33	55.4°	14.95 µH	-1173 Ω
6.0	3.69	66.1°	15.37 µH	-1084 Ω
6.78	3.30	67.0°	15.31 µH	-1062 Ω
8.0	2.79	69.6°	15.20 µH	-991 Ω
10.0	2.17	72.3°	14.97 µH	-845 Ω
12.0	1.75	73.3°	14.50 µH	-680 Ω
13.57	1.52	73.6°	13.94 µH	-537 Ω
14.0	1.46	73.8°	13.77 µH	-494 Ω
16.0	1.23	74.6°	12.66 µH	-280 Ω
18.0	1.05	72.4°	12.06 µH	-69 Ω
20.0	0.88	19.6°	11.30 µH	+199 Ω



Frequency shift.wmf

Figure 4-4 Frequency shift of the oscillator as a function of the impedance X_C of the pulling Capacitor C6 on the application board

The frequency of the reference crystal oscillator is being pulled by the capacitor C6. Figure 4-4 shows the pulling effect by C6 for a frequency of 13.56MHz. C6 has been grounded at one side for this test. The diagram shows the frequency pulling effect as a function of the impedance X_C of the pulling capacitor. The values given have been taken on the evaluation board for a crystal having typical dynamic parameters.

They include the effect of the spurious capacity of the crystal to ground of 2.2pF. The reference frequency in the diagram (at 0 ppm) is specified as the resonance frequency of the crystal for the specified load capacitance of C_L = 20pF. As can be seen, the pulling range is quite large. This is typical for an oscillator circuit representing an inductive component to the crystal. The further the frequency is pulled down however, the more the frequency stability will degrade. As a design rule, the frequency should not be pulled down too far.

This keeps the frequency tolerance and the temperature drift, caused by the characteristics of the internal inductive component of the TDA5100 (not including the crystal itself), low.

The total capacitive load to the oscillator port should be kept below 10pF. Otherwise spurious oscillation may arise at the resonance frequency of this capacitance with the internal inductive component of the TDA5100.

The design of the oscillator circuit can be implemented on the basis of the above information. As a practical design rule Figure 4-4 can be used to find the values of C6 and C7 and the ordering specification of the crystal.

For ASK operation of the transmitter, C7 will be replaced by a short. C6 can be grounded then, and pin11 can be left open. As a first design step, C6 can be calculated from Table 4-2. The effective load-impedance represented to the crystal is given by adding the impedances of C6 and the internal inductance of the oscillator circuit as given in Table 4-2. C6 has to be chosen to sum up with the internal inductance to the designed load capacitance of the crystal. To compensate for the parasitics, a fine tuning of C6 has to be done for the final layout on the PCB.

Design Example:	
Transmit frequency	868.40 MHz
Modulation	ASK
Crystal	$f_c = f_{tx}/64 = 13.56875$ MHz, load capacitance $C_L = 20$ pF, fundamental mode

According to Table 4-2, the inductance of the oscillator circuit under max. load conditions is $L_{XO} = 13.94\ \mu H \cong + j1188\ \Omega$. Loaded with a high-Q-crystal, the inductance will rather be $10.5\ \mu H \cong + j895\Omega$. The designed load capacitance of the crystal is $C_L = 20pF \cong -j586\Omega$. So, the effective capacitance to be placed in series with the crystal will be given by:

$$X_C = -j895\ \Omega\ -j586\ \Omega\ = -j1481\Omega$$
$$C\ =\ 7.92\ pF$$

The stray capacitance of the crystal to ground is 2.2 pF in total. Adding half of it at each port of the crystal to the oscillator circuit will give a final value of C6 of

$$C6\ =\ 6.5\ pF$$

A more accurate design of C6 can be done on produced basis of Figure 4-4. This function has been taken for different values of C6 from the evaluation board. It therefor includes all the parasitics to be effective on the board.

According to Figure 4-4, C6 has to be

$$X_{C6} = -j1440\ \Omega$$
$$C6 = 8.15\ pF$$

to get the oscillator to the designed resonance frequency of the crystal.

As can be seen from Figure 4-4, the slope of the graph at the resonance point is +180 ppm/kΩ. Thus, a variation of the capacitance by ± 0.1pF ≅ ± j20 Ω results in a frequency offset error of ± 3.6 ppm ≅ ± 3.1 kHz at a frequency of 869MHz.

FSK modulation is achieved by frequency modulation of the reference oscillator. The switch at FSKOUT, pin11 is operated by the modulating signal, being DC coupled. During the closed state the frequency-determining capacitor is C6. During the open state a capacitor C7 is added in series with C6, increasing the frequency by an amount equal two times the frequency shift. The On/Off state of the switch at pin11 has the characteristic impedance of:

Z_{on} :	120 Ω // 6pF	(for 6.8MHz)
	120 Ω //3.5pF	(for 13.57MHz)
Z_{off} :	12kΩ // 2.5pF	

A logic high at the FSK input FSKDTA pin7 results in an open switch and hence in a frequency being determined by C6 in series with C7. A logic low closes the switch and reduces the frequency to a value given by C6. As a first design step, the values for C6 and C7 giving the desired center frequency and frequency deviation can be taken from Figure 4-4.

The value of C6 can be found at a frequency higher than the center frequency by the designed frequency deviation. The value of C7 to be put in series with C6 will be found at the frequency point lower than the center frequency by the designed frequency deviation. In order to compensate for the parasitics of the PCB, a fine tuning of C6 and C7 has to be done for the final layout on the board.

Design Example:	
Transmit frequency	868.40 MHz
Modulation	FSK, frequency deviation ± 20kHz
Crystal	$f_c = f_{tx}/64$ = 13.56875 MHz, load capacitance C_L = 20pF ≅ -j586 Ω, fundamental mode

The lower frequency state is determined by C6. This frequency should be lower than the center frequency by the designed frequency deviation of -20 kHz/868.4 MHz = -23ppm. As can be seen from Figure 4-4, the capacitor C6 will be

X_{C6} = -j1.44 kΩ + j1kΩ * 23ppm/180ppm = -j1.32 kΩ

C6 = 8.88 pF.

At the high frequency state the shift by +46ppm related to the lower frequency state will be given by adding a capacitor of

$$X_{C7} = -j1\ k\Omega * 46ppm/180ppm = -j255\ \Omega$$
$$C7 = 46\ pF$$

in series with C6. Subtracting the capacitance of the open switch at pin 10 yields

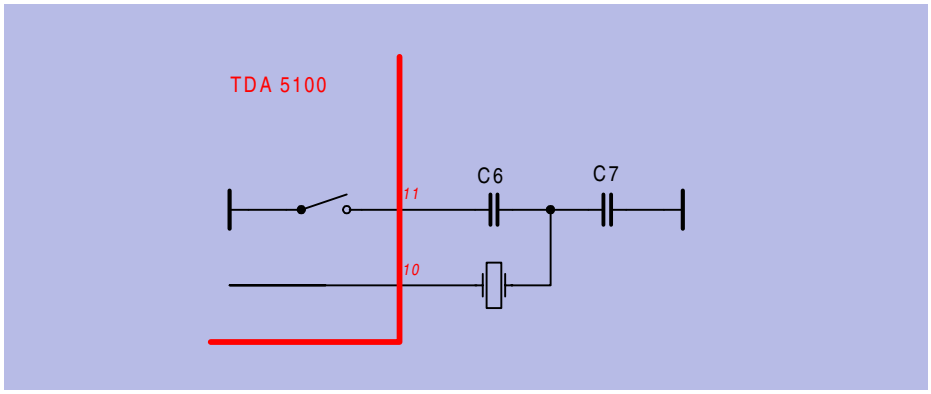
$$C7 = 46\ pF - 2.5\ pF = 43.5\ pF$$

Both the design examples for ASK and for FSK modulation have been done for a crystal being specified for a load capacitance of C_L=20 pF. This specification is well suited for a reliable design of the reference oscillator. The range of C_L is limited by the practicability of the capacitors C6 and C7 and the susceptability of the oscillator to induced noise for too low values. The resultant values for C6 and C7 can be obtained with low tolerances. The capacitor C6 determines the center frequency of the transmitter. It can be specified for a tolerance of ± 0.1 pF. It has been shown that this will result in a frequency error of ± 3.1 kHz at a frequency within the 869MHz band.

All the above calculations have been done for the more economical crystals in the 13.57 MHz frequency range. The design rules can be applied to crystals at 6.8 MHz as well.

As a general and more practical design rule for C6 and C7, the following procedure may apply:

- Choose a crystal for the designed frequency with a nominal load capacitance of CL=10pF to CL=20pF.
- Determine the value of C6 on the board for a documented crystal to get the designed carrier frequency for a transmitter being ASK-modulated.
- For a transmitter being FSK-modulated, C6 has to be chosen to get a frequency lower than the carrier frequency by the designed frequency deviation. The FSK switch (pin11) has to be kept closed during this process. While the FSK switch is open, C7 will be added to give a frequency just higher than the designed carrier frequency by the FSK frequency deviation.
- If the capacitance of C6 and C7 can not be realized by standard values, adding two capacitors in series or in parallel will give a combination which allows a tuning-free design.
- This procedures applies for crystals at 6.8 MHz and 13.7 MHz.



Inverted_fsk.wmf

Figure 4-5 Inverted FSK

According to Figure 4-5, the phase of modulation can be inverted by switching a capacitor C6 in parallel with C7 and not in series. This design is recommended for systems operating at a large FSK frequency deviation. The oscillator is more equally stable then for both the frequency states. The phase of the baseband signal in the receiver has to be adapted to the transmitted signal.

4.3 Frequency stability

The frequency stability of the transmitter is affected by a number of factors:

- Tuning tolerance of the crystal
- Temperature stability of the crystal
- Aging of the crystal
- Tuning tolerance of the oscillator circuit
- Tuning stability of the oscillator circuit
- Detuning of the oscillator due to nearby obstacles
- Detuning of the oscillator due to RF feedback
- Operating voltage
- Temperature stability of the oscillator circuit

In the following table an assessment of the worst case overall frequency spread to be expected in case of operation at 868MHz with a 13.56875MHz Tokyo Denpa reference crystal as denoted in the Bill of Materials in Table 4-3 is shown. The calculation is taking into account the tolerance of the crystal and of the components in the oscillator circuit which are determining the tuning tolerance and temperature stability of the circuit. Note that the result is a sum of the squares of the indivual terms.

A spreadsheet[1] may be obtained from Infineon which can be used to predict the total frequency error under worst-case conditions by simply entering the crystal specification.

Table 4-3 Assessment of the Worst Case Frequency Error of the Crystal Oscillator

Tolerance of the crystal	spread of nominal frequency ± 20ppm	± 20ppm
	temperature stability ±20ppm	± 20ppm
Tolerance of the circuit	tolerance of the series load capacitor C_V ±2%	±8ppm
	tolerance of the oscillator circuit (3 σ spread of internal component values assumed), calculated with spreadsheet	±48ppm
	Total frequency spread under worst-case conditions	± 63ppm

1.available for download on the Infineon RKE Webpage www.infineon.com/rke, also included on evalkit CD-ROM

4.4 Modulation

A stand alone encoder device has been imparted to the transmitter board. The encoder chip HCS 360 (Microchip) is used as a signal source to modulate the transmitter either in ASK or in FSK mode. The code-hopping data sequence of the HCS 360 is band-limited by an RC low pass filter (4.7 kΩ with 4.7 nF) at a cutoff frequency of 7.2 kHz before it is applied to the modulation input of the TDA 5100.

The logic of the power-up function at the modulation inputs of the TDA 5100 allows some different modes of interfacing to the encoder and the actuator key. Power-down mode at a very low standby current will be held if both the ASK and the FSK modulation inputs (pin6 and pin7) and the PDWN input, pin 1 are at a low state. A high state at the PDWN input will power up the internal device. A logic high or an open at one of the modulation inputs will internally supply a pullup current to the PDWN input. This will power up the device under an open condition at the PDWN input. A low at the PDWN input, pin 1 will force the device to the off state. The supply current will be 40µA then if one of the modulation input is at a logic high state.

Mode of Operation	PDWN Input	Modulation Input	
		ASKDTA	FSKDTA
Power down	L, open	L	L
Off State	L	H	H
CW, carrier	H, open	H	H, L, open
ASK	H, open	Data	H
FSK	H, open	H	Data

The low voltage detect output will be pulled down if the supply voltage falls below the trigger level of 2.15 V. The output configuration is a open collector common emitter stage. It can be used as a warning input signal to the controller or to shut down the transmitter if a critical low voltage situation is reached. In both modes of modulation the shut-off function can be easily realized by pulling down the ASK modulation input by the low voltage detect signal. A series resistor will decouple the output to the encoder.

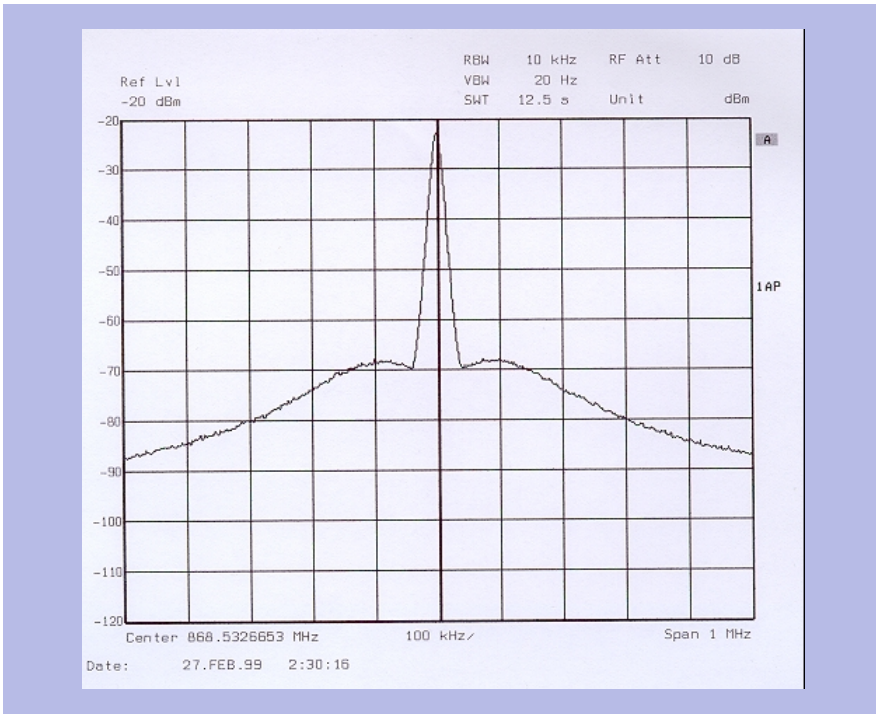
The interface circuit on the evaluation board had to be adapted to the specific encoder being used. Pin6 of the encoder chip has to be kept at a low state during the power-up sequence. This avoids blocking of the encoder due to a false signal at its I/O pin6 during power-up.

Load pulling of the VCO frequency by the PA will result in quite some residual FSK modulation when the PA is ASK modulated. The frequency deviation will be as much as 3MHz peak. The duration of this frequency step is limited by the reaction time of the PLL to app. 10µs. The output spectrum of the transmitter will show some spurious content within a band of ±3MHz to the carrier frequency. The spectral density will increase with higher ASK data rates.

In order to comply with the regulations for spurious emition, the data rate as to be kept below 10KB/s in practice.

The noise spectrum of the transmitter at a carrier frequency at 869MHz is shown in Figure 4-6.

It is measured with a resolution bandwidth of 10 kHz. It shows the typical noise suppression within the loop bandwidth of 150 kHz. Sideband noise of the VCO outside the loop bandwidth at ± 200 kHz can be specified at -91dBc/Hz.



Noise_869.wmf

Figure 4-6 Noise spectrum at 869MHz

4.5 Lock time

The lock-up time of the transmitter includes both the start-up time of the crystal oscillator and the PLL lock time. The circuit has been designed to minimize both times.

The time constant of the start-up process of the reference oscillator is given by

$$\tau = 2Q / \Delta v\, \omega$$

As can be seen, the start-up time $t_S \approx 20 * \tau$ is inversely proportional to the bandwidth of the crystal. A 13.5 MHz oscillator therefore will start twice as fast as a 6.7 MHz oscillator assuming a constant crystal Q. By using a 13.5 MHz crystal and the 64 prescaler, the start-up time of the crystal oscillator can be cut in half over that achieved by the 6.7MHz crystal oscillator circuit. As can be seen from Table 2-1, the excessive gain Δv of the oscillator has been designed for a very high value within the TDA 5100. Experimentally, a power-up start-up time for the oscillator of T_S= 600 µs has been recorded using 13.5 MHz crystals.

The PLL lock time t_L is related to the PLL natural frequency ω_n by

$$t_L \approx 10 / \omega_n$$

The internal loop filter to the TDA 5100 has been designed for a natural frequency of

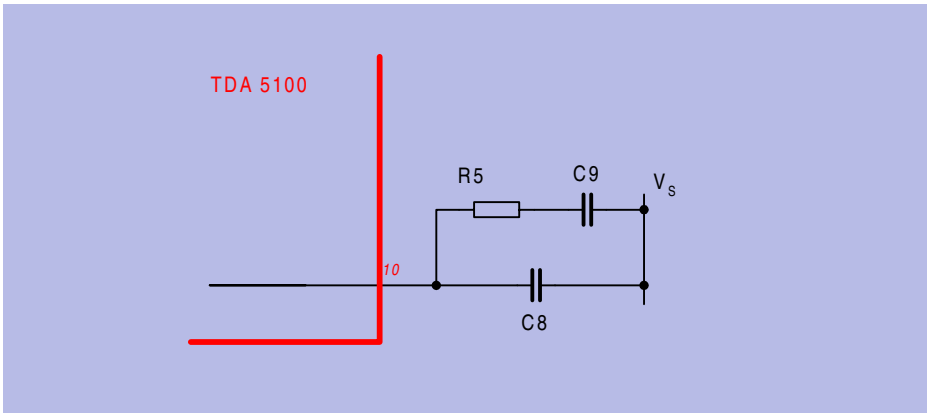
$$\omega_n = 2\pi\ 150\ \text{kHz}.$$

The resultant lock time will be $t_L \approx 10$ µs.

To obtain maximum flexibility in the system design the characteristics of the loop can be modified externally by adding a second-order RC loop filter. As can be seen from Figure 4-7 it consists of two capacitors and a resistor in a shunt configuration at pin4. It will reduce the natural loop frequency to a design value.

The characteristic parameters of the PLL are:

VCO tuning sensitivity	K_{VCO} =	55 MHz / V
Phase detector gain	K_Φ =	30 µA / rad
Division ratio	N =	64 (13.5MHz)
	N =	128 (6,8 MHz)



External_loop.wmf

Figure 4-7 Optional external loop filter for reduced loop bandwidth

FSK modulation is imparted directly to the reference oscillator. The VCO has to be fast enough to follow the frequency variations within the loop. As the primary consideration, the modulation rate needs to be much lower than the PLL bandwidth to enable the PLL to track the modulation. In practice, the PLL bandwidth should be at least five to ten times higher than the maximum data rate input to the modulator.

4.6 Clock output

The clock output CLKOUT, pin 8 can be configured to supply a clock signal to a microcontroller. The frequency of the clock signal is fixed to the values:

Table 4-4

Clock frequency	CLKDIV input
3.39 MHz	Low
847.5 kHz	High (or open)

The clock output is a open collector configuration. This will reduce DC power consumption to zero if it is not used. A external pull up resistor R_{CL} has to be applied to drive the clock input of the microcontroller. It has to be designed to drive the effective load capacitance C_{CL} (microcontroller input and wiring capacitance) at a low to high signal transition:

$$R_{CL} \leq 1 / 8*C_{CL}*f_{CL}$$

R_{CL} should be designed as high as possible in order to reduce overall DC power consumption.

5 Reference

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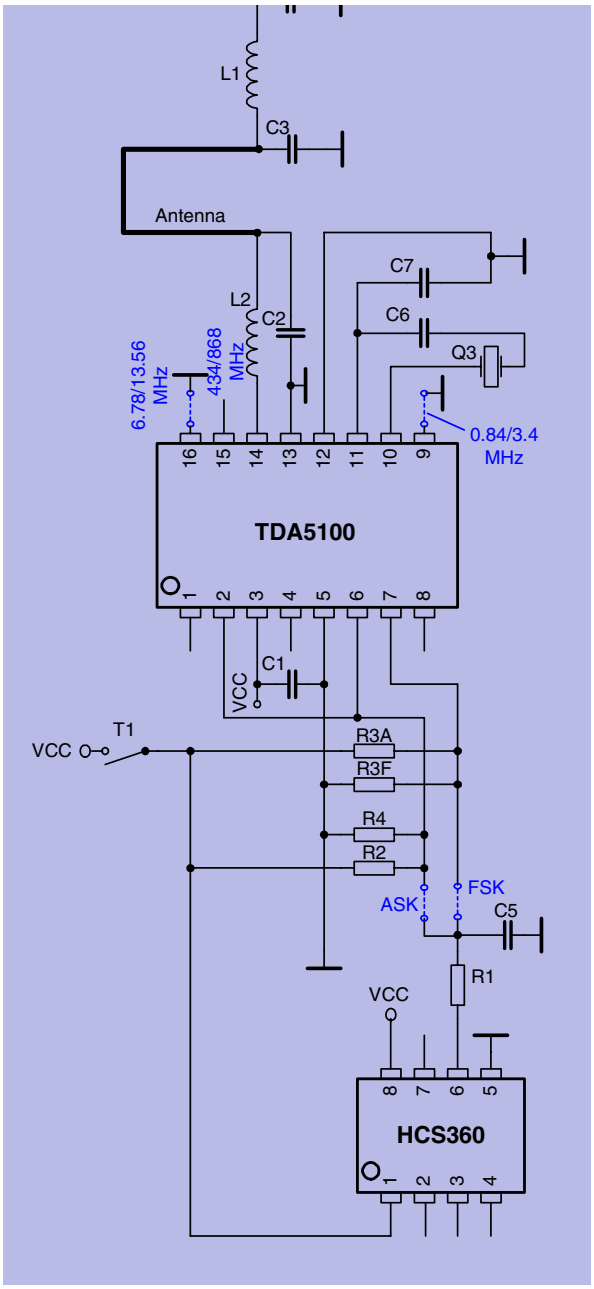
5.1 Application Circuit



Application_circuit.wmf

Figure 5-1 Application Circuit

5.2 Test Board Layouts

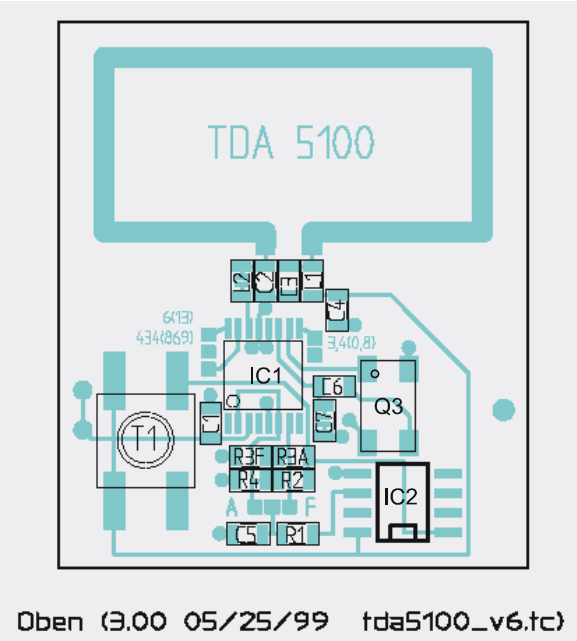


Figure 5-2 Top Side of TDA 5100

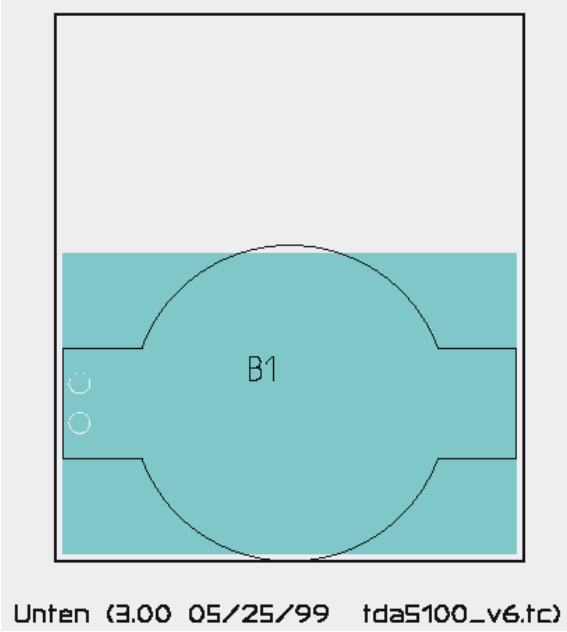


Figure 5-3 Bottom Side of TDA 5100

5.3 Bill of material (Application Circuit)

Table 5-1 Bill of material

Part	Value	434 MHz	869 MHz	ASK	FSK	Specification
R1	4.7 kΩ					0805, ± 5%
R2					12 kΩ	0805, ± 5%
R3A				15 kΩ		0805, ± 5%
R3F					15 kΩ	0805, ± 5%
R4	15 kΩ					0805, ± 5%
C1	47 nF					0805,X7R, ± 10%
C2		8.2 pF	1.5 pF			0805, COG, ± 5%
C3		4.7 pF	1.0 pF			0805, COG, ± 0.1 pF
C4	100 pF					0805, COG, ± 5%
C5	4.7 nF					0805,X7R, ± 10%
C6	8.2 pF					0805, COG, ± 0.1 pF
C7		22 pF	47 pF	0Ω		0805, COG, ± 5% 0805 0Ω Jumper
L1		100 nH	27 nH			TOKO LL2012-J
L2		0Ω	22 nH			0Ω resistor bridge 22nH: TOKO LL1608-J
Q3	13.56875 MHz CL=20pF					Tokyo Denpa TSS-3B 13568.75kHz Spec.No. 20-18906
IC1	TDA5100					
IC2	HCS360					Microchip
B1	Batteriehalter					HU2031-1, RENATA
T1	Taster					STTSKHMPW, ALPS

5.4 Application Board

V6_photo.wmf

Figure 5-4 Photo of Application Board TDA5100