ANALOG DEVICES

AN-392
APPLICATION NOTE

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Circuit Design and Applications of the ADM663A/ADM666A Micropower Linear Voltage Regulators

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GENERAL INFORMATION

The ADM663A/ADM666A contains a micropower bandgap reference voltage source; an error amplifier, A1; three comparators, C1, C2, C3, and a series pass output transistor. A P-channel FET and an NPN transistor are used on the ADM663A while the ADM666A uses an NPN output transistor.

CIRCUIT DESCRIPTION

The internal bandgap reference is trimmed to 1.3 V ± 30 mV. This is used as a reference input to the error amplifier A1. The feedback signal from the regulator output is supplied to the other input by an on-chip voltage divider or by two external resistors. When V_{SET} is at ground, the internal divider tap between R1 and R2, provides the error amplifier's feedback signal giving a +5 V output. When V_{SET} is at V_{IN}, the internal divider tap between R2 and R3 provides the error amplifier's feedback signal giving a +3.3 V output. When V_{SET} is at more than 50 mV above ground and less than 50 mV below V_{IN}, the error amplifier's input is switched directly to the V_{SET} pin, and external resistors are used to set the output voltage. The external resistors are selected so that the desired output voltage gives 1.3 V at V_{SET}.

Comparator C1 monitors the output current via the SENSE input. This input, referenced to $V_{OUT(2)}$, monitors the voltage drop across a load sense resistor. If the voltage drop exceeds 0.5 V, then the error amplifier A1 is disabled and the output current is limited.

The ADM663A has an additional amplifier, A2, which provides a temperature proportional output, V_{TC}. If this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The ADM666A has an additional comparator, C4, that compares the voltage on the low battery input, LBI, pin to the internal +1.3 V reference. The output from the comparator drives an open drain FET connected to the low battery output pin, LBO. The low battery threshold may be set using a suitable voltage divider connected to LBI. When the voltage on LBI falls below 1.3 V, the open drain output LBO is pulled low.

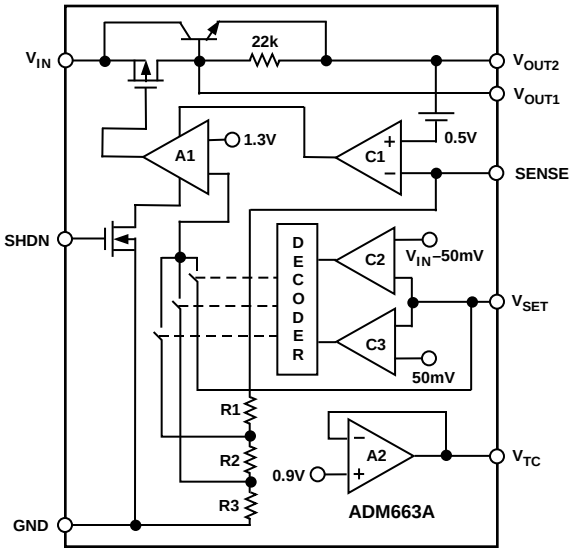

Figure 1. ADM663A Functional Block Diagram

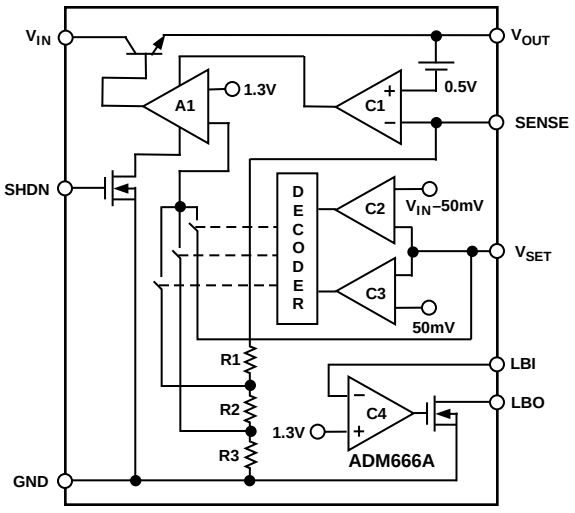

Figure 2. ADM666A Functional Block Diagram

Both the ADM663A and the ADM666A contain a shutdown (SHDN) input that can be used to disable the error amplifier and hence the voltage output. The power consumption in shutdown reduces to less than 9 μA.

Circuit Configurations

For a fixed +5 V output the V_{SET} input is grounded and no external resistors are necessary. This basic configuration is shown in Figure 3. For a fixed +3.3 V output, the V_{SET} input is connected to V_{IN} as shown in Figure 4. Current limiting is not being utilized so the SENSE input is connected to $V_{OUT(2)}$.

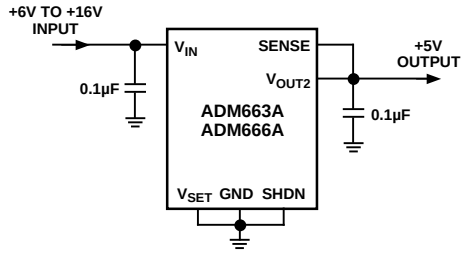

Figure 3. A Fixed +5 V Output

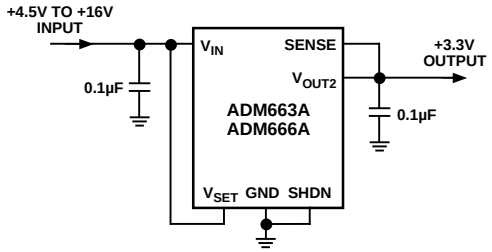

Figure 4. A Fixed +3.3 V Output

Output Voltage Setting

If V_{SET} is not connected to GND or to V_{IN}, the output voltage is set according to the following equation:

$$V_{OUT} = V_{SET} \times \frac{(R1 + R2)}{R1}$$

where V_{SET} = 1.30 V.

The resistor values may be selected by first choosing a value for R1 and then selecting R2 according to the following equation:

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30} - 1 \right)$$

The input leakage current on V_{SET} is 10 nA maximum. This allows large resistor values to be chosen for R1 and R2 with little degradation in accuracy. For example, a 1 MΩ resistor may be selected for R1, and then R2 may be calculated accordingly. The tolerance on V_{SET} is guaranteed at less than ±30 mV so in most applications, fixed resistors will be suitable.

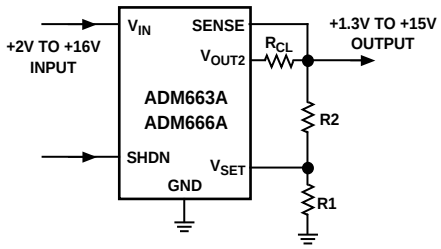

Figure 5. Adjustable Output

Table I. Output Voltage Selection

V_{SET}	V_{OUT}
GND	+5 V
V_{IN}	+3 V
R1/R2	ADJ

Current Limiting

Current limiting may be achieved by using an external current sense resistor in series with $V_{OUT(2)}$. When the voltage across the sense resistor exceeds the internal 0.5 V threshold, current limiting is activated. The sense resistor is therefore chosen such that the voltage across it will be 0.5 V when the desired current limit is reached.

$$R_{CL} = \frac{0.5}{I_{CL}}$$

where R_{CL} is the current sense resistor, I_{CL} is the maximum current limit.

The value chosen for R_{CL} should also ensure that the current is limited to less than the 100 mA absolute maximum rating and also that the power dissipation will also be within the package maximum ratings.

If current limiting is employed, there will be an additional voltage drop across the external sense resistor that must be considered when determining the regulators dropout voltage.

If current limiting is not used, the SENSE input should be connected to $V_{OUT(2)}$. In this case, input current should be limited so that in case of short circuited output, device power dissipation does not exceed the rated maximum.

Shutdown Input (SHDN)

The SHDN input allows the regulator to be turned off with a logic level signal. This will disable the output and reduce the current drain to a low quiescent (9 μA maximum) current. This is very useful for low power applications. The SHDN input should be driven with a CMOS logic level signal since the input threshold is 0.3 V. In TTL systems, an open collector driver with a pull-up resistor may be used.

If the shutdown function is not being used, then it should be connected to GND.

Low Supply or Low Battery Detection

The ADM666A contains on-chip circuitry for low power supply or battery detection. If the voltage on the LBI pin falls below the internal 1.3 V reference, then the open drain output LBO will go low. The low threshold voltage may be set to any voltage above 1.3 V by appropriate resistor divider selection.

$$R3 = R4\left(\frac{V_{BATT}}{1.3\,V} - 1\right)$$

where R3 and R4 are the resistive divider resistors and V_{BATT} is the desired low voltage threshold.

Since the LBI input leakage current is less than 10 nA, large values may be selected for R3 and R4 in order to minimize loading. For example, a 6 V low threshold may be set using 10 M Ω for R3 and 2.7 M Ω for R4.

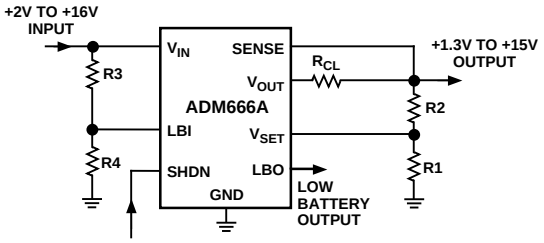

Figure 6. ADM666A Adjustable Output with Low Battery Detection

Low Output Detection

The circuit in Figure 7 will generate a low LBO when output voltage drops below a preset value determined by the following equations:

$$R2 + R3 = R1\left(\frac{V_{OUT}}{1.3} - 1\right)$$

$$R3 = (R1 + R2)\left(\frac{V_{OL}}{1.3} - 1\right)$$

for V_{OUT} = 5.0 V nominal, V_{OL} = 3% of V_{OUT} = 4.85 V and R1 = 1 MΩ solving the equations simultaneously we will get R2 = 31 kΩ and R3 = 2.82 M Ω.

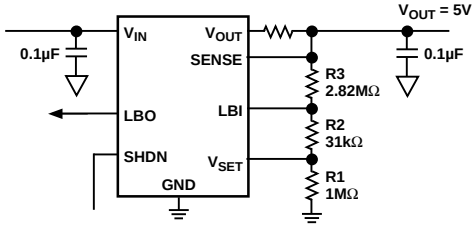

Figure 7. Voltage Regulator Circuit with Low Output Detector

High Current Operation

The ADM663A contains an additional output, V_{OUT1}, suitable for directly driving the base of an external NPN transistor. Figure 8 shows a configuration which can be used to provide +5 V with boosted current drive. A 1 Ω current sensing resistor limits the current at 0.5 A.

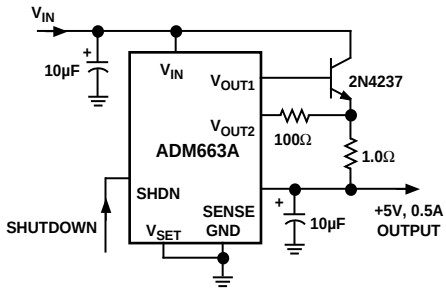

Figure 8. ADM663A Boosted Output Current (0.5 A)

Temperature Proportional Output

The ADM663A contains a V_{TC} output with a positive temperature coefficient of +2.5 mV/ °C typ. This may be connected to the summing junction of the error amplifier (V_{SET}) through a resistor resulting in a negative temperature coefficient at the output of the regulator. This is especially useful in multiplexed LCD displays to compensate for the inherent negative temperature coefficient of the LCD threshold. At +25 °C, the voltage at the VTC output is typically 0.9 V. The equations for setting both the output voltage and the tempco are given below. If this function is not being used, then V_{TC} should be left unconnected.

$$V_{OUT} = V_{SET}\left(1 + \frac{R2}{R1}\right) + \frac{R2}{R3}(V_{SET} - V_{TC})$$

$$TCV_{OUT} = \frac{-R2}{R3}(TCV_{TC})$$

where V_{SET} = +1.3 V, V_{TC} = +0.9 V, TCV_{TC} = +2.5 mV/°C

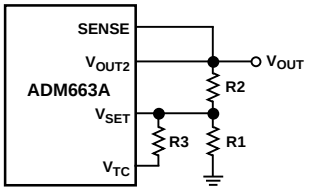

Figure 9. ADM663A Temperature Proportional Output

APPLICATION HINTS

Input-Output (Dropout Voltage)

A regulator's minimum input-output differential or dropout voltage determines the lowest input voltage for a particular output voltage. The ADM663A/ADM666A dropout voltage is 1 V at 100 mA output current. For example when used as a fixed +5 V regulator, the minimum input voltage is +6 V. At lower output currents (I_{OUT} < 10 mA) on the ADM663A, V_{OUT1} may be used as the output driver in order to achieve lower dropout voltages. In this case the dropout voltage depends on the voltage drop across the internal FET transistor. This may be calculated by multiplying the FET's saturation resistance by the output current, for example with V_{IN} = 9 V, R_{SAT} = 20 Ω. Therefore, the dropout voltage for 5 mA is 100 mV. As the current limit circuitry is referenced to V_{OUT2}, V_{OUT2} should be connected to V_{OUT1}. For high current operation V_{OUT2} should be used alone and V_{OUT1} left unconnected.

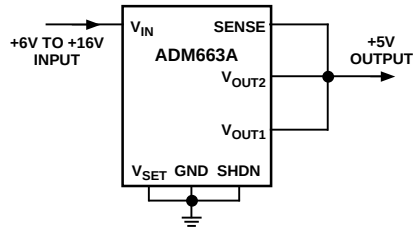

Figure 10. Low Current, Low Dropout Configuration

Thermal Considerations

The ADM663A/ADM666A can supply up to 100 mA load current and can operate with input voltages up to 16.5 V, but the package power dissipation and hence the die temperature must be kept within the maximum limits. The package power dissipation is calculated from the product of the voltage differential across the regulator times the current being supplied to the load. The power dissipation must be kept within the maximum limits given in the Absolute Maximum Ratings section.

$$P_D = (V_{IN} - V_{OUT})\ (I_L)$$

The die temperature is dependent on both the ambient temperature and on the power being dissipated by the device. The ADM663A/ADM666A contains an internal thermal limiting circuit which will shut down the regulator if the internal die temperature exceeds 125 °C. Therefore, care must be taken to ensure that, under normal operating conditions, the die temperature is kept below the thermal limit.

$$T_J = T_A + P_D\ (\theta_{JA})$$

This may be expressed in terms of power dissipation as follows:

$$P_D = (T_J - T_A)/(\theta_{JA})$$

where:

T_J = Die Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipation (W)

θ_{JA} = Junction to Ambient Thermal Resistance (°C/W)

If the device is being operated at the maximum permitted ambient temperature of +85 °C, the maximum power dissipation permitted is:

$$P_D\ (max) = (T_J\ (max) - T_A)/(\theta_{JA})$$

$$P_D\ (max) = (125 - 85)/(\theta_{JA})$$

$$= 40/\theta_{JA}$$

θ_{JA} = 120 °C/W for the 8-pin DIP (N-8) package
θ_{JA} = 170 °C/W for the 8-pin SOIC (R-8) package

Therefore, for a maximum ambient temperature of 85 °C

$$P_D\ (max) = 333\ mW\ for\ N\text{-}8$$

$$P_D\ (max) = 235\ mW\ for\ R\text{-}8$$

At lower ambient temperatures the maximum permitted power dissipation increases accordingly up to the maximum limits specified in the absolute maximum specifications.

The thermal impedance (θ_{JA}) figures given are measured in still air conditions and are reduced considerably where fan assisted cooling is employed. Other techniques for reducing the thermal impedance include large contact pads on the printed circuit board and wide traces. The copper will act as a heat exchanger thereby reducing the effective thermal impedance.

High Power Dissipation Recommendations

Where excessive power dissipation due to high input-output differential voltages and or high current conditions exists, the simplest method of reducing the power requirements on the regulator is to use a series dropping resistor. In this way the excess power can be dissipated in the external resistor. As an example, consider an input voltage of +12 V and an output voltage requirement of +5 V @ 100 mA with an ambient temperature of +85 °C. The package power dissipation under these conditions is 700 mW which exceeds the maximum ratings. By using a dropper resistor to drop 4 V, the power dissipation requirement for the regulator is reduced to 300 mW which is within the maximum specifications for the N-8 package at +85 °C. The resistor value is calculated as R = 4/0.1 = 40 Ω. A resistor power rating of 400 mW or greater may be used.

Bypass Capacitors

The high frequency performance of the ADM663A/ADM666A may be improved by decoupling the output using a filter capacitor. A capacitor of 0.1 μF is suitable.

An input capacitor helps reduce noise, improves dynamic performance and reduces the input dV/dt at the regulator input. A suitable input capacitor is 0.1 μF or greater.

Typical Performance Characteristics

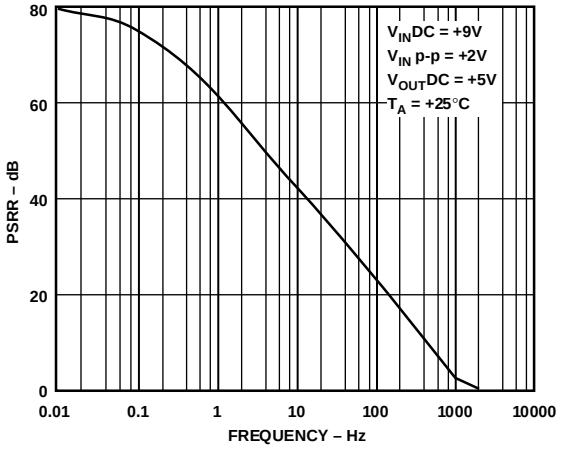

Figure 11. Power Supply Rejection Ratio vs. Frequency

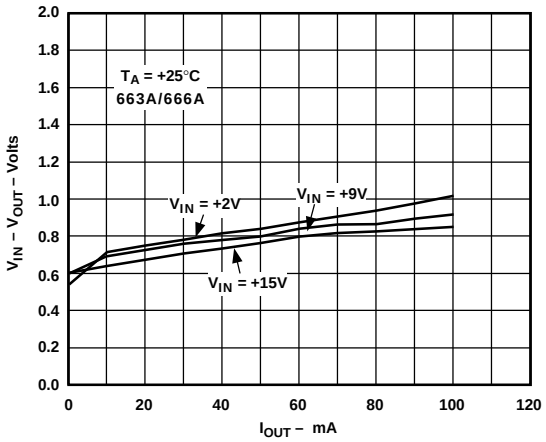

Figure 14. ADM663 V_{OUT2}, ADM666 Input-Output Differential vs. Output Current

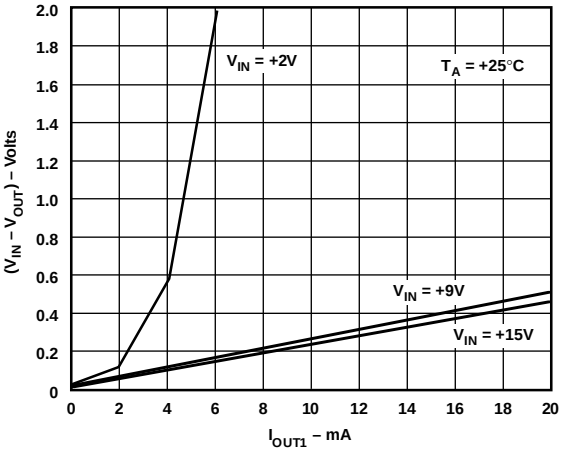

Figure 12. ADM663A V_{OUT1} Input-Output Differential vs. Output Current

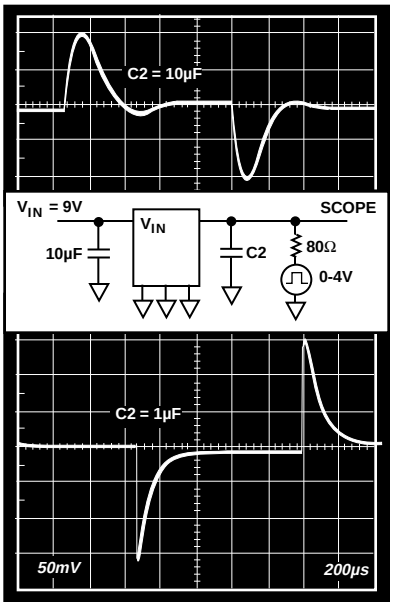

Figure 15. Load Transient Response

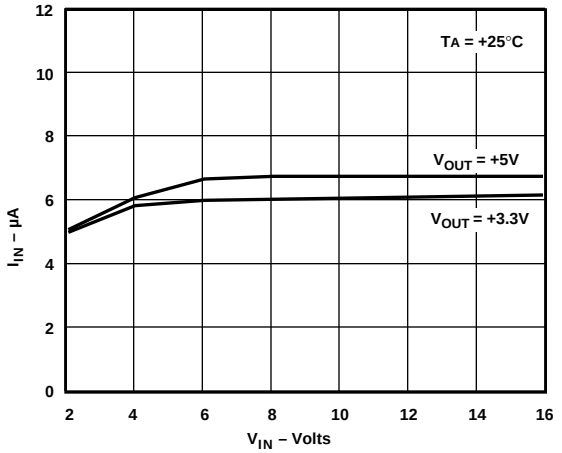

Figure 13. Quiescent Current vs. Input Voltage

2.0A LDO Voltage Regulator with Short Circuit Protection

In battery powered systems, battery life is significantly affected by the voltage regulator's dropout voltage. These systems often require low dropout linear regulators capable of high output current and extremely low quiescent current.

The circuit in Figure 16 can source current in excess of 2 A with less than 400 mV dropout voltage and consumes less than 10 µA in shutdown mode. The c ircuit exhibits excellent line and load regulation and better than 5% initial output voltage accuracy.

Unlike other LDO voltage regulators which require large capacitors in excess of 10 µF for stability, a very small 0.1 µF bypass capacitor is sufficient for this circuit.

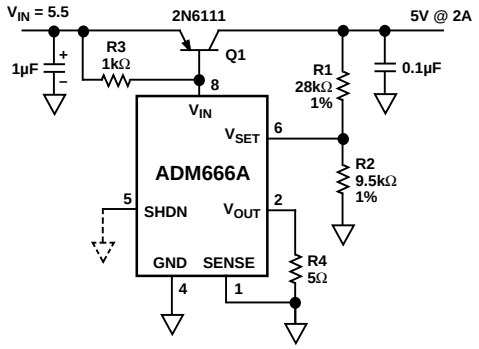

Figure 16. 2.0A LDO Regulator

The circuit's maximum current is determined by the selection of the pass transistor's current gain, ß, and its maximum power dissipation. For low dropout voltage, a viable choice is a PNP pass transistor with appropriate power dissipation and ß. The s implified functional diagram in Figure 17 helps clarify the circuit's operation.

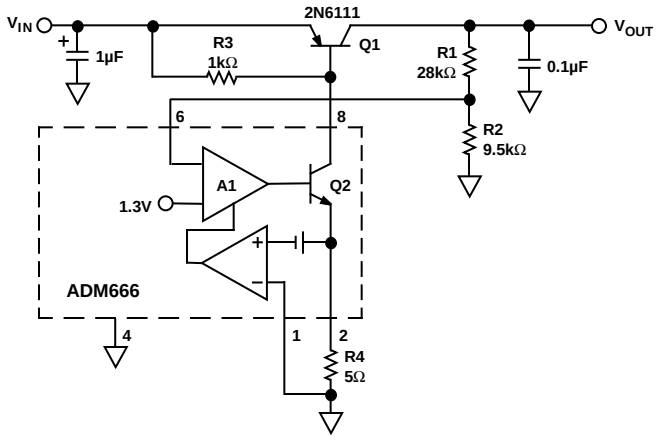

Figure 17. Simplified Functional Diagram

The 2N6111 is in a servo loop with ADM666A's voltage reference, error amplifier and driver circuit.

To maintain regulation, output voltage is continuously monitored by comparing the voltage on the set pin (Pin 6) to a 1.3 V internal voltage reference. The difference is amplified by the error amplifier, A1, and used to control the pass transistor's base current, thus controlling its collector current. As output voltage changes due to a change in input voltage or load current, the pass transistor's base current is adjusted to maintain a constant output voltage.

Since maximum base current is limited to ADM666A's, short circuit current set by R4 to 100 mA, pass transistors with higher ß will source higher currents to the load. As a result, output short circuit current behavior of the circuit depends on the pass transistor's ß.

Another significant advantage of using a pass transistor with high ß is to achieve higher efficiency since most of the input current is diverted to the load and only a small fraction of it is used to control the servo loop.

For high current applications where low dropout voltage is not required, a power Darlington transistor can be substituted to take advantage of its relatively high ß. The trade-off of this approach is higher power dissipation due to Darlington's high saturation voltage.

Output voltage is programmable between 1.3 V to 15.4 V by selecting appropriate resistor values for the voltage divider network using the following equation:

$$V_{OUT} = 1.3\,V\left(\frac{R1+R2}{R2}\right)$$

The circuit's performance is shown in Figures 18 and 19.

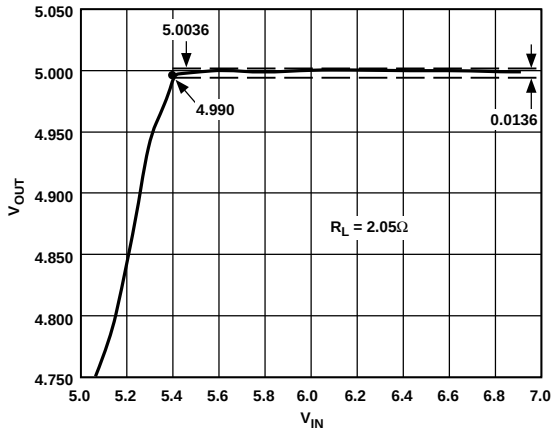

Figure 18. Output Voltage vs. Input Voltage

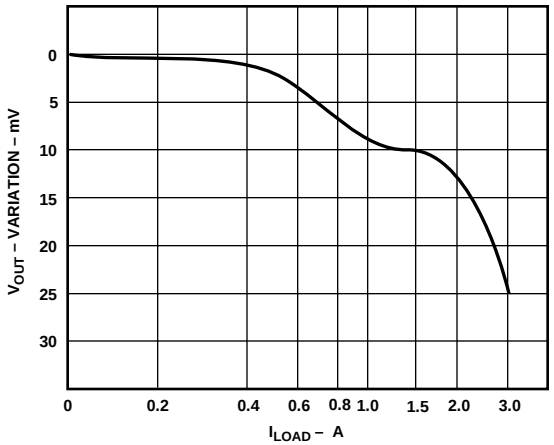

Figure 19. Output Voltage Variation vs. Load Current

The short circuit current is limited by limiting the pass transistor's base current, I_b to a value determined by:

$$I_b = \frac{0.5}{R4}$$

The actual value of the short circuit current is determined by the ß of the pass transistor which in this case is in 30 to 150 range at a collector current of 3.0 A dc.

For more accurate short circuit current control, the circuit in Figure 20 is a simple way to add short circuit protection.

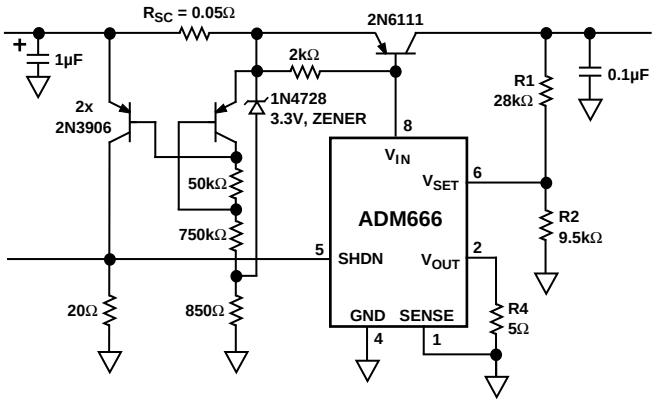

Figure 20. External Short Circuit Protection

The short circuit current is determined by using the following equation:

$$R_{SC} = \frac{0.1}{I_{SC}}$$

An appropriate heat sink must be utilized to avoid damage to the pass transistor as well as controller IC. Figure 21 is a plot of the current through the controller and voltage across it vs. input voltage at a constant load current.

As the curve indicates, maximum power dissipation for controller occurs when input voltage is between 5.4 V to 5.6 V, worst case being 215 mW at V_{IN} = 5.53 V, which is well within the product specification.

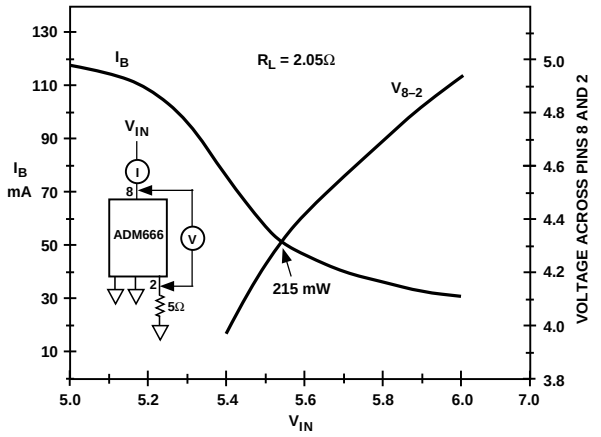

Figure 21. Controller IC Power Dissipation

However, the pass transistor requires adequate heat sink specially if it were to operate with large input output voltage differential.

LDO Regulator with Battery Crossover Switch

The circuit in Figure 22 automatically connects the standby battery to the circuit when primary voltage source is disconnected or drops below a preset voltage level.

Battery ON voltage level is determined using the following equation:

$$R1 = R2\left(\frac{(V_{BAT})}{1.3\,V} - 1\right)$$

An N-channel power FET switch with very low R_{ON} is used to achieve a very low dropout across the switch when it is ON.

Optional resistor R3 is used to compensate for constant losses by self-discharge or trickle charging of the battery. Consult the battery specification to determine trickle charge current and maximum permissible over charge current.

Resistor values used in this circuit are optimized for low power operation, when monitoring BAT-ON output; avoid excessive loads on this output.

Shut-down pin should be tied to ground if it is not used.

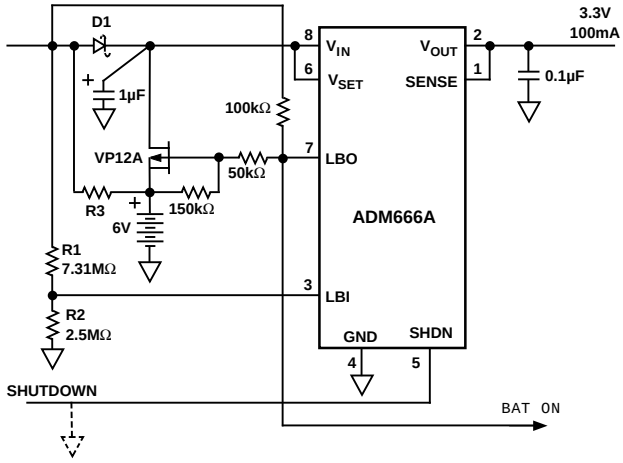

Figure 22. LDO Regulator with Battery Crossover Switch Circuit

Low Battery Disconnect Circuit

To prevent damage to the battery and loss of data due to battery over-discharge, the circuit illustrated in Figure 23 monitors the battery voltage and disconnects the battery from the circuit when it drops below a preset value.

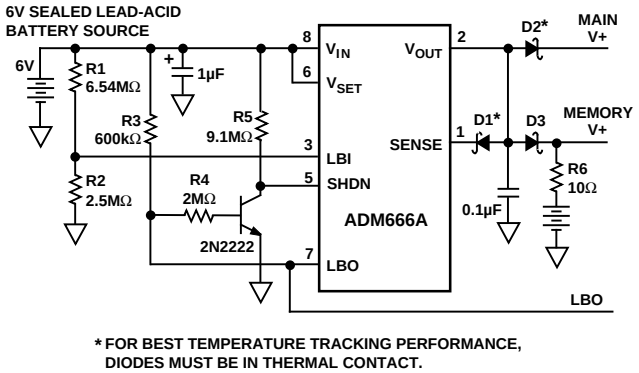

Figure 23. Low Battery Disconnect and Memory Backup Circuit

Diode D2 is added for isolation; D1 is to compensate for voltage drop across D2. For better output voltage accuracy performance, diodes D1 and D2 must be in thermal contact. Surface mount Schottky diodes mounted in close proximity of each other offer the best temperature tracking performance.

In battery disconnect mode, the circuit's quiescent current is less than 20 µA. If LBO function is not needed or it is monitored via a high impedance input, the circuit's current consumption can be reduced significantly by replacing R4 with a short and R3 with a 9 MΩ resistor. This circuit has less than 10 µA quiescent current.

5 Volt Supply with Battery Backup and Battery ON Lag

The circuit in Figure 24 switches to NiCd backup battery when the main input voltage drops below value set by R1, R2 and R3 and returns to the main input when its voltage reaches the preset value set by R3.

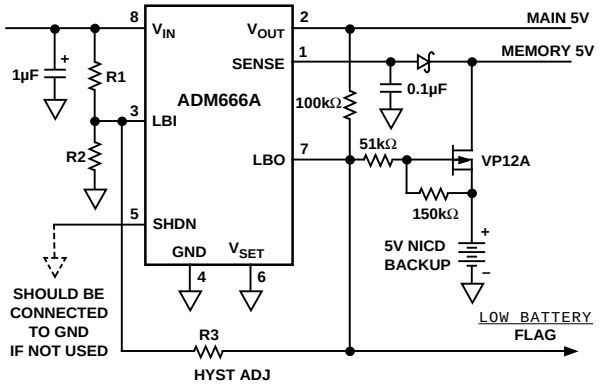

Figure 24. 5 V Battery Powered Supply with Backup and Battery ON Flag

The Battery ON flag goes low whenever the circuit is switched to NiCd battery.

Low Cost Battery Charger Circuits

A simple, low cost and yet flexible battery charger is presented in Figure 25. Maximum output voltage is programmed by selection of R1 and R2 ratio's using

$$R1 = R2\left(\frac{(V_{OUT})}{1.3V} - 1\right)$$

for V_{OUT} = 7.8 V, R1 = 2.82 MΩ, and R2 = 560 kΩ. Maximum charge current is determined by the current limiting resistor which in this case is 100 mA set by R8.

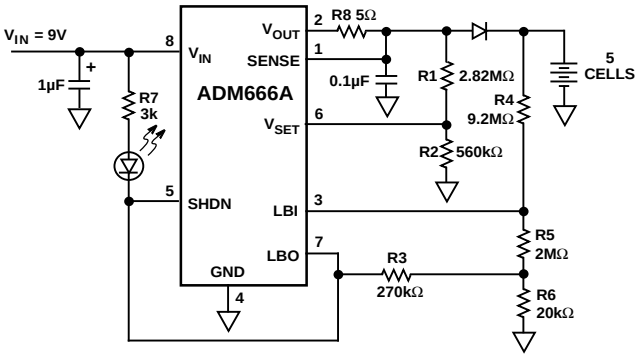

Figure 25. Low Cost Battery Charger

Charge termination voltage, V_T, and charge resume voltage, V_{CH}, are set by R3, R4 and R5. Charging is terminated when battery voltage reaches V_T.

Charge termination voltage, which in this case is 7.2 V, is calculated using the following equation:

$$R4 = (R5 + R6)\left[\frac{V_T}{1.3} - 1\right]$$

where R6 = 20 kΩ, and R4 = 9.2 MΩ.

ADM666A continues to monitor the battery voltage level; charging will resume when it drops below the V_{CH}.

The V_{CH} level is set by adjusting R3.

With resistor values selected in Figure 26, charging starts when the battery voltage is around V_{CH} = 5 volts and will terminate when the battery voltage reaches slightly above 7.2 V.

Charger status is indicated by the LED. A lighted LED indicates charger ON; a flashing LED indicates battery disconnect.

To minimize calculation errors and maximize the circuit efficiency, LED current should be limited to about 2 mA.

To minimize current drain by battery voltage monitoring circuit's, large resistor values are selected for R4 and R5 (see text for recommended values).

Charge current is limited to 100 mA by a short circuit current limiting resistor. However higher charge current is possible using the circuit in Figure 26.

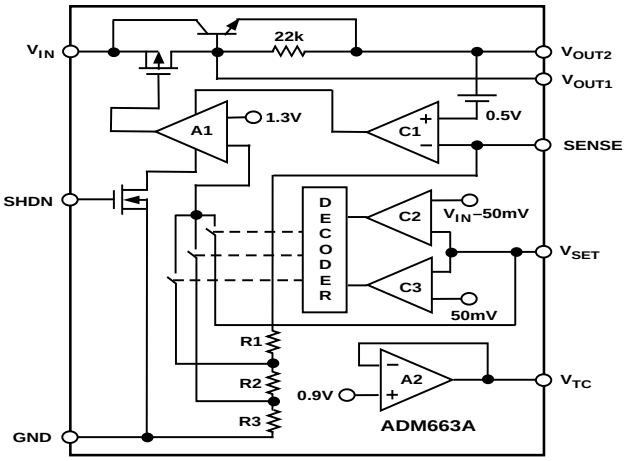

Figure 26. High Charge Current Battery Charger

Power PNP pass transistor with appropriate current rating is controlled by the ADM666A.

Available charge current is determined by the transistor's power rating, its current gain, ß, and controlled by the short circuit current limit resistor.

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